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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,824	09/25/2003	Daniel Alan Brokenshire	AUS920030702US1	7306

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EXAMINER	
NGUYEN, PHILLIP H	

ART UNIT	PAPER NUMBER
2191	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,824	BROKENSHIRE ET AL.	
	Examiner	Art Unit	
	Phillip H. Nguyen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2003,2005,2006,2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on 5/20/2007.

2. Claims 1, 2, 7, 11, 12, 17, 21-23, 25 and 27-30 have been amended.

3. Claims 1-30 have been considered below.

Specification

4. The amendment filed on 5/20/2007 overcomes the rejection to the specification for using trademark (JAVA) without capitalized or without a proper trademark symbol, such as TM of previous action. Therefore, the rejection is withdrawn.

Drawings

5. The amendment filed on 5/20/2007 overcomes the objection to the drawings of previous action. Therefore, the objection is withdrawn.

Claim Objections

6. The amendment filed on 5/20/2007 overcomes the objection to claim 11 of previous action. Therefore, the objection is withdrawn.

Double Patenting

7. Applicant asserts on page 15 of the amendment that a terminal disclaimer has been submitted to overcome the double patenting rejection. However, Examiner

notices that a terminal disclaimer has not been submitted. Therefore, Examiner maintains the double patenting rejection.

8. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

9. Claim 11 is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 17 of copending Application No. 10/670,835. Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications use steps that are clearly similar. For instance, in claim 1, feature (f) of instant application states, "identifying one of the processor to execute a software task, the identification based upon characteristics of the software task and computing resource availability" while the copending application no. 10/670,835 recites, "signal, from the first processor, the second processor".

Although, the copending application no. 10/670,835 does not explicitly disclose "identifying one of the processor to execute a software task..." However, it is obvious to one of ordinary skill in the art to recognize that the processors are identified as first processor and second processor and the second processor is the identified processor that executes (processes) the code (data).

The following tables show few claims to demonstrate the reason for rejection.

Application No. 10/670,824	Application No. 10/670,835
11. An information handling system comprising: a) a plurality of heterogeneous processors; b) a common memory shared by the plurality of heterogeneous processors; c) a first processor selected from the plurality of processors that sends a request to a second processor, the second processor also being selected from the plurality of processors; d) a local memory corresponding to the second processor; e) a DMA controller associated with the second processor, the DMA controller adapted to transfer data between the	17. An information handling system comprising: a) a plurality of heterogeneous processors; b) a common memory shared by the plurality of heterogeneous processors; c) a first processor selected from the plurality of processors that sends a request to a second processor, the second processor also being selected from the plurality of processors; d) a local memory corresponding to the second processor; e) a DMA controller associated with the second processor, the DMA controller adapted to transfer data between the

common memory and the second processor's local memory; and f) a loading tool for loading software code to execute on one of the processors, the loading tool including software effective to: i) identifying one of the processor to execute a software task, the identification based upon characteristics of the software task and computing resource availability; ii) loading the software code corresponding to the identified processor into the common memory; and iii) executing the loaded code by the identified processor.	common memory and the second processor's local memory; and f) a virtual device tool for operating the second processor as a virtual device, the virtual device tool including software effective to: i) signal, from the first processor, the second processor; ii) store data corresponding to the request in the second processor's local; and iii) process the data by the second processor using software code stored in the second processor's local memory.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Arguments

10. Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1, 8-11, 18-21 and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Washington et al. (United States Patent No.: 5,835,775).

As per claims 1 and 21

Washington discloses:

- identifying a processor to execute a software task, the identification based upon characteristics of the software task and computing resource availability (see at least col. 4, lines 35-37 "**The CPU test section 210 includes routines for determining which type of processor of a processor family is executing the FGPS file 200**");
- loading software code corresponding to the identified processor into a shared memory, wherein the shared memory is shared by a plurality of dislike processors that includes the identified processor (see at least col. 5, lines 47-48 "**transfers the FGPS file 200 from the mass storage device 108 to the main memory 106**"); and

- executing the loaded code by the identified processor (see at least col. 5, lines47-48 "**schedules the process of executing the FGPS file 200 to the first processor 102**").

As per claims 8, 18 and 28:

Washington further discloses:

- signaling the identified processor (see at least col. 5, lines47-48 "**schedules the process of executing the FGPS file 200 to the first processor 102**" – This is similar to signaling the first processor to execute FGPS file 200; also see col. 10, lines 46-50 "**task switching between different processor types**..." – This also considered as signaling the second processor for continue processing the task);
- reading, by the identified processor, the software code from the shared memory into a local memory corresponding to the identified processor (see at least col. 8, lines 11-12 "**allocates at least one page of main memory 106 to each processor of the computer system 100**"); and
- executing the software code by the identified processor (see at least col. 5, lines47-48 "**schedules the process of executing the FGPS file 200 to the first processor 102**").

As per claims 9, 19 and 29:

Washington further discloses:

- writing an instruction block in the shared memory (see at least col. 5, lines 47-48 "**transfers the FGPS file 200 from the mass storage device 108 to the main memory 106**"), the instruction block including the address of the loaded software code and the address of an input buffer (see at least col. 7, lines 1-5 "**FGPS file 400 contains...the file header 408 may contain information such as a file type identifier (e.g. an identifier representing a FGPS file type), a pointer to the section header table 416, the address of the FGPS file 400 to begin execution, etc.**"); and
- reading the software code and the input buffer from the locations identified in the instruction block to the identified processor's local memory (see at least col. 8, lines 11-12 "**allocates at least one page of main memory 106 to each processor of the computer system 100**").

As per claims 10, 20 and 30:

Washington further discloses:

- signaling the identified processor from one of the other processors (see at least col. 10, lines 46-50 "**task switching between different processor types**..." – This also considered as signaling the second processor for continue processing the task), the signaling including:

- writing the address of the instruction block to a mailbox that corresponds to the identified processor (**the address of the instruction block must be written to the memory area 502 or 504 of the processors**); and
- reading, by the identified processor, the instruction block in response to the signal (see at least col. 10, lines 44-45 "**the second processor resumes the execution of the FGPS file 400**").

As per claim 11:

Washington further discloses:

- a plurality of heterogeneous processors (see at least col. 3, lines 64-65 "**a hybrid multiprocessors**");
- a common memory shared by the plurality of heterogeneous processors (see at least col. 8, lines 16 "**shared memory area 56**");
- a first processor selected from the plurality of processors that sends a request to a second processor, the second processor also being selected from the plurality of processors (see at least col. 10, lines 46-50 "**to enable task switching between different processor types, the operating system may only stop the execution...resumed on a processor of different type**" – when task switching between processors, the first processor must send request to second processor for continuing the execution of a task);
- a local memory corresponding to the second processor (see at least col. 8, line 11-13 "**allocates at least one page of main memory 106 to each processor of**

the computer system 100" – the idea is to allocate a memory area for each processor);

- a DMA controller associated with the second processor, the DMA controller adapted to transfer data between the common memory and the second processor's local memory (**the operating system program is use for transferring data**); and
- a loading tool for loading software code to execute on one of the processors, the loading tool including software effective to:
    - identify one of the processors to execute a software task, the identification based upon characteristics of the software task and computing resource availability (see at least col. 4, lines 35-37 "**The CPU test section 210 includes routines for determining which type of processor of a processor family is executing the FGPS file 200**");
    - loading the software code corresponding to the identified processor into the common memory (see at least col. 5, lines 47-48 "**transfers the FGPS file 200 from the mass storage device 108 to the main memory 106**"); and
    - executing the loaded code by the identified processor (see at least col. 5, lines47-48 "**schedules the process of executing the FGPS file 200 to the first processor 102**").

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 2-7, 11-17 and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washington et al. (United States Patent No.: 5,835,775).

As per claims 2, 12 and 22:

Washington does not explicitly discloses:

- prior to the identifying, compiling a source program into at least two object files, each executed on a different processor selected from the plurality of dislike processors, wherein the software code that is loaded and executed is one of the object files.

However, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to recognize that compiling a source program into two object files and each adapted to be executed on a different processor is well known to the relevant art. One would have been motivated to create two separate object files for each different processor for simplification purposes. Another words, one big file is more complicated comparing to multiple smaller files.

As per claims 3, 13 and 23:

Washington further discloses:

- analyzing the source program for program characteristics (see at least col. 5, lines 50-52 "**executes the processor test section 210 which returns an identifier representing the processor type of the first processor 102**" – meaning, analyzing the processor test section 210 of the FGPS file to get a processor identifier); and
- storing the program characteristics (see at least col. 5, lines 58-59 "**causes this identifier to be stored in the processor type flag 212**").

As per claims 4, 14 and 24:

Washington further discloses:

- wherein at least one of the program characteristics is selected from the group consisting of data locality, computational intensity, and data parallelism (**identifier represents the type of processor that is executing the FGPS file**).

As per claims 5, 15 and 25:

Washington further discloses:

- retrieving the program characteristics (see at least col. 5, lines 50-52 "**executes the processor test section 210 which returns an identifier representing the processor type of the first processor 102**");

Washington does not explicitly disclose:

- retrieving current system characteristics, wherein the current system characteristics includes processor load characteristics for the plurality of dislike processors; and
- combining the program characteristics and the current system characteristics to determine which of the dislike processors to assign the software task.

However, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify Washington's approach to include system characteristics for identifying processor to execute FGPS file. One would have been motivated to maintain current system characteristics for the plurality of dislike processor for identifying which of the dislike processors is suitable for executing the FGPS file.

As per claims 6, 16 and 26:

Washington further discloses:

- wherein at least one of the current system characteristics is selected from the group consisting of processor availability for each of the dislike processors, and a data size of data being processed by the software task (see at least col. 3, lines 64-65 "**a hybrid multiprocessor computer system**").

As per claims 7, 17 and 27:

Washington further discloses:

- determining that the identified processor has a scheduler that schedules tasks for the processor (see at least col. 4, lines 45-50 "**the operating system program**

as a result of receiving a request to execute the FGPS file 200 transfers the FGPS file 200 from the mass storage device 108 to the main memory 106 and schedules the process of executing the FGPS file 200..." – the operating system program is a scheduler for scheduling tasks for the processors).

Washington does not explicitly disclose:

- scheduling the software code to execute on the identified processor, the scheduling including:
    - writing a software code identifier corresponding to the software code to a run queue corresponding to the identified processor.

However, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify Washington's approach to write identifier of the processor to a run queue in stead of memory whenever is needed. One would have been motivated to modify because saving the software code identifier in a run queue is saving more memory space.

As per claim 11:

Washington further discloses:

- a plurality of heterogeneous processors (see at least col. 3, lines 64-65 "**a hybrid multiprocessors**");
- a common memory shared by the plurality of heterogeneous processors (see at least col. 8, lines 16 "**shared memory area 56**");

- a first processor selected from the plurality of processors that sends a request to a second processor, the second processor also being selected from the plurality of processors (**even if Washing fails to teach this limitation, it would have been obvious to one having an ordinary skill in the art at the time the invention was made to modify Washington's approach to allow the first processor sends a request to the second processor when task switching takes place. One would have been motivated to send a request to the second processor to indicate that referencing a virtual address not within the first page of the common code section to allow the second processor to step in to resume the execution of the FGPS file**);
- a local memory corresponding to the second processor (see at least col. 8, line 11-13 "**allocates at least one page of main memory 106 to each processor of the computer system 100**" – the idea is to allocate a memory area for each processor);
- a Direct Memory Access (DMA) controller associated with the second processor, the DMA controller transferring data between the common memory and the second processor's local memory (**the operating system program is use for transferring data**); and
- a loading tool to load software code to execute on one of the processors, the loading tool including software effective to:
    - identify one of the processors to execute a software task, the identification based upon characteristics of the software task and computing resource

availability (see at least col. 4, lines 35-37 "**The CPU test section 210 includes routines for determining which type of processor of a processor family is executing the FGPS file 200**");

- loading the software code corresponding to the identified processor into the common memory (see at least col. 5, lines 47-48 "**transfers the FGPS file 200 from the mass storage device 108 to the main memory 106**"); and
- executing the loaded code by the identified processor (see at least col. 5, lines47-48 "**schedules the process of executing the FGPS file 200 to the first processor 102**").

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Smith et al. (US 6,049,668).
- McCrory Duane (US 6,513,057).
- Fish et al. (US 6,381,693).
- Ansari et al. (US 6,473,897).
- Morris Dale (US 7,080,242).
- Zimmer et al. (US 7,134,007).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip H. Nguyen whose telephone number is (571) 270-1070. The examiner can normally be reached on Monday - Thursday 10:00 AM - 3:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PN
7/27/2007

WEI ZHEN
SUPERVISORY PATENT EXAMINER